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09/964,315	09/26/2001	Shakuntala Anjanaiah	TI-31779	9921

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2189	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/964,315	ANJANAIAH ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-20 and 22 are presented for examination. Claim 2 was cancelled by the amendment filed May 26, 2005. Claim 21 was cancelled by the amendment filed August 29, 2006.

SPECIFICATION

2. The objection to the 'RELATED APPLICATIONS' section of the disclosure is ***withdrawn*** due to the amendment.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

CLAIM OBJECTIONS

4. The objection to claim 12 is ***withdrawn*** due to the amendment.

DOUBLE PATENTING

5. The rejections given previously for provisional double patenting are ***maintained*** from the last office action.

35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

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7. Claims 1, 3-20 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by McWilliams.

8. McWilliams teaches the invention (claim 1) as claimed including a data processing system comprising:

a communication bus as part of the communication network (e.g., see paragraph 0026);

a plurality of data processing units, the data processing units including:

a central processing unit (e.g., see Figure 3);

a direct memory access unit coupled to the central processing unit (e.g., see Figure 3);

a Utopia mode interface unit coupled to the direct memory access unit, the Utopia interface unit acting in a receive mode and in a transmit mode as a UTOPIA to LVDS bridge device (e.g., see Figure 3);

the Utopia transfer mode interface unit having:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals (e.g., see paragraph 0027);

a buffer memory unit, the buffer memory unit buffering data signals between the direct memory access unit and the processor as a multi-port buffers (e.g., see Figure 3); and,

wherein one or the data processing units operates in a master mode and the remainder of the data processing units operate in a slave mode (e.g., see paragraph 0043).

As to claim 3, McWilliams teaches the buffer memory unit is a first-in-first-out memory unit

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As to claim 4, McWilliams teaches the processor includes:

an input interface unit, an output interface unit (e.g., see Figure 3);

wherein the buffer memory unit includes:

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal and an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal (e.g., see Figure 3 and paragraph 0159).

As to claim 5, McWilliams teaches data is transferred from the communication bus to the input buffer memory unit, and wherein data is transferred from the output buffer memory unit to the communication unit through the output interface unit (e.g., see Figure 3).

As to claim 6, McWilliams teaches the input buffer memory unit and the output buffer memory units are first-in-first-out memory units (e.g., see paragraph 0159).

As to claim 7, McWilliams teaches the receive event signal is generated when the buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the buffer memory unit and the direct memory access unit is begun and wherein the transmit event signal is generated when the buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun (e.g., see Figure 3 and paragraph 0159).

As to claim 22, McWilliams teaches the transfer of data cells between the buffer memory unit and the direct memory interface units determined by an event signal, the event signal

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indicating to the direct memory access unit that a data cell is stored in the buffer memory unit in the receive mode, the event signal indicating to the direct memory access unit that space for a data cell is available in buffer memory unit in the transmit mode (e.g., see Figure 3 and paragraph 0159).

9. McWilliams teaches the invention (claim 8) as claimed including a data processing system including a communication bus for exchanging asynchronous transfer mode protocol signals, and a plurality of data processing units, the data processing units having:

a central processing unit (e.g., see Figure 3);

a direct memory access unit coupled to the central processing unit (e.g., see Figure 3);

a Utopia interface unit coupled between the direct memory access unit (e.g., see paragraph 0159);

the Utopia interface unit comprising:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals (e.g., see paragraph 0027);

a buffer memory unit, the buffer memory unit buffering data signals between the direct memory access unit and the processor, an event signal indicating to the direct memory access unit when a data cell has been received by the buffer memory unit in a receive mode, an event signal indicating to the direct memory access unit that space for a data cell is available in the receive mode (e.g., see Figure 3); and ,

wherein the Utopia interface unit can send and receive signals in either the master-mode or the slave-mode (e.g., see paragraph 0043).

As to claim 9, McWilliams teaches the processor includes:

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an input interface unit; an output interface unit (e.g., see Figure 3);

wherein the buffer memory unit includes;

an input buffer memory unit and an output buffer memory unit (e.g., see Figure 3).

As to claim 10, McWilliams teaches the data is transferred from the communication bus through the input interface unit to the input buffer memory unit, and wherein data is transferred from the output buffer memory unit through the output interface unit to the communication bus (e.g., see paragraph 0027).

As to claim 11, McWilliams teaches the input buffer memory unit and the output buffer memory unit are first-in-first-out memory units (e.g., see Figure 3 and paragraph 0159).

10. McWilliams teaches the invention (claim 12) as claimed including an Utopia interface unit for providing an interface between an external data processing unit and a direct memory access unit, the interface unit comprising:

an input buffer memory unit, the input buffer memory unit providing data cells to the direct memory interface unit, the input buffer unit applying an event signal to direct memory access unit indicating that space is available for a data cell in a transmit mode, the input buffer applying an event signal to the direct memory access unit indicating that data cell is stored therein in a receive mode (e.g., see paragraph 0159);

an interface input unit, the interface input unit controlling the transmission of data cells form the external processing system to the input buffer memory unit (e.g., see Figure 3);

an output buffer memory unit, the output buffer memory unit receiving data cells from the direct memory access unit (e.g., see Figure 3);

an interface output unit, the interface output unit controlling transmission of data cells

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from the output buffer memory unit to the external processing system (e.g., see Figure 3);

wherein the interface unit can operate in either a master-mode or a slave-mode with respect to the external data processing unit (e.g., see paragraph 0043).

As to claim 13, McWilliams teaches the input buffer memory unit and the output buffer memory unit are first-in-first-out memory units (e.g., see paragraph 0159).

As to claim 14, McWilliams teaches the first-in-first-out memory units can store at least two data cells (e.g., see paragraph 0159).

As to claim 15, McWilliams teaches data from the input buffer memory unit is transferred to the direct memory access unit in response to word-read signal from the buffer memory unit (e.g., see paragraph 0159).

As to claim 16, McWilliams teaches data from the direct memory unit is stored in the output buffer memory unit in response to a word-write signal from the output buffer memory unit (e.g., see paragraph 0159).

As to claim 17, McWilliams teaches data is transferred from the external processing unit to the input buffer unit in response to the cell-available signal from the input buffer unit (e.g., see paragraph 0159).

As to claim 18, McWilliams teaches data is transferred from the output buffer memory unit to the external processing unit in response to the cell-available signal from the output buffer memory unit (e.g., see paragraph 0159).

As to claim 19, McWilliams teaches the interface unit is operation in a slave mode, the transfer of data cells from the input buffer memory unit and the direct memory access unit being determined by a receive event signal, the transfer of data cells from the direct memory access

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unit to the output buffer memory unit being determined by a transmit event signal (e.g., see 0043).

As to claim 20, McWilliams teaches the receive event signal is generated when the input buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the input buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the output buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the output buffer memory unit form the direct memory access unit is begun (e.g., see Figure 3 and paragraph 0159).

35 USC § 103

11. The rejection of claims 1, 3-20 and 22 as being unpatentable over Sun et al. in view of Miller et al. is ***maintained*** and updated to reflect the amendment.

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1 and 3-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al. in view of Miller et al.

14. Sun teaches the invention (claim 1) as claimed including a data processing system comprising:

a communication bus (e.g., see Figure 1);

a plurality of data processing units as hardware units attached to the SAR IC (e.g., see

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Figure 1 and col. 1, line 5 to col. 2, line 55);

a central processing unit (e.g., see Figure 1 and col. 1, line 5 to col. 2, line 55);

a direct memory access unit coupled to the central processing unit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53);

a Utopia mode interface unit coupled to the direct memory unit, the Utopia interface unit acting in a receive mode and in a transmit mode (e.g., see Figure 1 elements 120 and 140) the Utopia transfer mode interface unit having:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals therewith (e.g., see Figure 1 and col. 1, line 5 to col. 2, line 55); and,

a buffer unit for buffering data signals between the direct memory access unit and the processor, wherein the transfer of data cells between the buffer memory unit and the direct memory interface unit is determined by an event signal (e.g., see Figure 1); wherein one of the data processing units operates in a master mode and the remainder of the data processing units operate in a slave mode (e.g., see Figure 1 and col. 2, line 26 to page 3, line 2).

Sun teaches the limitations of the claim as given above, however, the reference does not teach details now claimed in relationship to the event signal. Miller teaches the same basic system with additional teachings related to signals for the transmit and receive buffers. Miller teaches the event signal as a signal as a RX status descriptor or as a transmit buffer descriptor (e.g., see col. 7, line 49 to col. 9, line 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaches of Miller with the teachings of Sun because both inventions are directed toward to the same system and have a common

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inventorship and a common assignee. Miller teaches using a UTOPIA interface unit thereby teaching the normal event or status signals while also teaching status signals for the buffer memory.

As to claim 3, Sun teaches the buffer memory unit is a first-in/first-out memory unit (e.g., see Figure 1, elements 120 and 140).

As to claim 4, Sun teaches an input interface unit and an output interface unit with the buffer memory unit includes:

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal (e.g., see Figure 1, elements 120 and 140 and Figure 3 and col. 4, line 25 to col. 6, line 21); and,

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal (e.g., see Figure 1, elements 120 and 140 and Figure 3 and col. 4, line 25 to col. 6, line 21).

As to claim 5, Sun teaches data is transferred from the communication bus to the input buffer memory unit and wherein data is transferred from the output buffer memory unit to the communication unit through the output interface unit

As to claim 6, Sun teaches the input buffer memory unit and the output buffer memory units are first-in/first-out memory units

As to claim 7, Sun teaches the receive event signal is generated when the buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the buffer memory unit and the direct memory access unit is begun as updating the RX status queue (e.g., see col. 7, line 49 to col. 8, line 6) and wherein the transmit event signal is

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generated when the buffer memory unit has space for a complete data cell as a transmit status descriptor (e.g., see col. 9, lines 1-17), the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun as signals for transmitting and receiving data using the receiving buffer and transmitting buffer which are present in the segmentation and reassembly (SAR) integrated circuit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53).

15. Sun teaches the invention (claim 8) as claimed including a data processing system including a communication bus for exchanging asynchronous transfer mode protocol signals and a plurality of data processing units (e.g., see Figure 1), the units comprising:

at least one slave-state data processing unit with the interface unit acting in either a master mode or a slave mode being a function of the UTOPIA protocol as stated in the background of the present invention section of the present disclosure at page 2, line 26 to page 3, line2, (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53);

a communication bus, the master-state data processing unit exchanging asynchronous transfer mode protocol signals with the bus (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53);

a master-state data processing unit, the master state data processing unit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53) including:

a central processing unit as being connected via the PCI bus to the SAR integrated circuit which has a memory interface (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53 and col. 6, lines 3-10);

a direct memory access unit coupled to the central processing unit (e.g., see col. 4,

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lines 33-47);

a Utopia interface unit coupled between the direct memory access unit (e.g., see Figure 1 and col. 5, line 5 to col. 6, line 10) with the Utopia interface unit having:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals therewith (e.g., see col. 5, line 5 to col. 6, line 10); and,

a buffer memory unit for buffering data signals between the direct memory access unit and processor (e.g., see col. 5, line 5 to col. 6, line 10); wherein the UTOPIA interface unit can send and receive signals in either the master-mode or the slave mode (e.g., see Figure 1).

Sun teaches the limitations of the claim as given above, however, the reference does not teach details now claimed in relationship to the event signal. Miller teaches the same basic system with additional teachings related to signals for the transmit and receive buffers. Miller teaches the event signal as a signal as a RX status descriptor or as a transmit buffer descriptor (e.g., see col. 7, line 49 to col. 9, line 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaches of Miller with the teachings of Sun because both inventions are directed toward to the same system and have a common inventorship and a common assignee. Miller teaches using a UTOPIA interface unit thereby teaching the normal event or status signals while also teaching status signals for the buffer memory.

As to claim 9, Sun teaches an input interface unit and an output interface unit with the buffer memory unit including an input buffer memory unit and an output buffer memory unit

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(e.g., see Figure 1).

As to claim 10, Sun teaches the data is transferred from the communication bus through the input interface unit to the input buffer memory unit and wherein data is transferred from the output buffer memory unit through the output interface unit to the communication bus (e.g., see Figure 1).

As to claim 11, Sun teaches the input buffer memory unit and the output buffer memory unit are first-in/first-out memory units (e.g., see Figure 1).

16. Sun teaches the invention (claim 12) as claimed including an Utopia interface unit for providing a interface between an external data processing unit and a direct memory access unit (e.g., see col. 5, line 5 to col. 6, line 10), the interface unit comprising:

an input buffer memory unit, the input buffer memory unit providing data cells to the direct memory interface unit (e.g., see col. 4, lines 33-47) the input buffer unit applying an event signal to direct memory access unit indicating that space is available for a data cell in a transmit mode (e.g., see col. 9, lines 1-17) the input buffer applying an event signal to the direct memory access unit indicating that data cell is stored therein in a receive mode (e.g., see col. 7, line 49 to col. 8, line 6);

an interface input unit, the interface input unit controlling the transmission of data cells from the external processing system to the input buffer memory unit (e.g., see Figure 1);

an output buffer memory unit for receiving data cells from the direct memory access unit (e.g., see col. 4, lines 33-47); and,

an interface output unit for controlling transmission of data cells from the output buffer memory unit to the external processing system (e.g., see Figure 1); wherein the interface unit can

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operate in either a master-mode or a slave-mode with respect to the external data processing unit (e.g., see Figure 1).

Sun teaches the limitations of the claim as given above, however, the reference does not teach details now claimed in relationship to the event signal. Miller teaches the same basic system with additional teachings related to signals for the transmit and receive buffers. Miller teaches the event signal as a signal as a RX status descriptor or as a transmit buffer descriptor (e.g., see col. 7, line 49 to col. 9, line 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaches of Miller with the teachings of Sun because both inventions are directed toward to the same system and have a common inventorship and a common assignee. Miller teaches using a UTOPIA interface unit thereby teaching the normal event or status signals while also teaching status signals for the buffer memory.

As to claim 13, Sun teaches the input buffer memory unit and the output buffer memory unit are first-in/first-out memory units (e.g., see Figure 1).

As to claim 14, Sun teaches the first-in/first-out memory units can store at least two data cells (e.g., see Figure 1).

As to claim 15, Sun teaches data form the input buffer memory unit is transferred to the direct memory access unit in response to word-read-signal from the buffer memory unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 16, Sun teaches data from the direct memory unit is stored in the output buffer memory unit in response to a word-write signal from the output buffer memory unit as

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signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 17, Sun teaches data is transferred from the external processing unit to the input buffer unit in response to the cell-available signal from the input buffer unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 18, Sun teaches data is transferred from the output buffer memory unit to the external processing unit in response to cell-available signal form the output buffer memory unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 19, Sun teaches the interface unit is operating in a slave mode, the transfer of data cells form the input buffer memory unit and the direct memory access unit being determined by a receive event signal, the transfer of data cells form the direct memory access unit to the output buffer memory unit being determined by a transmit event signal as signals for transmitting and receiving data using the receiving buffer and transmitting buffer which are present in the segmentation and reassembly (SAR) integrated circuit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53).

As to claim 20, Sun teaches the receive event signal is generated when the input buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the input buffer memory unit and the direct memory access unit is begun and wherein the transmit event signal is generated when the output buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the output buffer memory unit from the direct memory access unit is began as signals for

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transmitting and receiving data using the receiving buffer and transmitting buffer which are present in the segmentation and reassembly (SAR) integrated circuit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53).

As to claim 22, Miller teaches the transfer of data cells between the buffer memory unit and the direct memory interface unit is determined by an event signal as the Rx status queue (e.g., see Figure 3a, element 303), the event signal indicating to the direct memory access unit that a data cell is stored in the buffer memory unit in the receive mode, the event signal indicating to the direct memory mode, the event signal indicating to the direct memory access unit that space for a data cell is available in buffer memory unit in a transmit unit as updating the RX status queue (e.g., see col. 7, line 49 to col. 8, line 6) and wherein the transmit event signal is generated when the buffer memory unit has space for a complete data cell as a transmit status descriptor (e.g., see col. 9, lines 1-17), the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun.

RESPONSE TO APPLICANT'S REMARKS

17. Applicant's arguments filed August 29, 2006 have been fully considered but they are not persuasive.

18. As to the Sun reference not teaching the claimed invention, the applicant appears to be arguing how the present invention is implemented and used which is outside of the constraints of the actual claim language.

19. As to the reference using coprocessors and/or digital processing units, they units cited are performing the claimed functionality. The actual claim language does not preclude the use of such elements being read on the claimed limitations. The references are using the same

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communication bus for various functions in both the master-mode and slave-mode. There in an absence of sufficient detail in the claims for the claims for read over the references in regards to the use of a particular bus.

CONCLUSION

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Thursday, July 05, 2007

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